ABSTRACT OF THE DISCLOSURE

A method for parallel scrambling of a sequence of serially transmitted digital bits comprises an initializing scrambling step and subsequent scrambling step. The initializing scrambling step comprises the steps of generating a scrambling bit sequence and storing the scrambling bit sequence in a scrambling register. The subsequent scrambling step comprises:

storing a sequential group of bits in the same sequence in which they were received , each of the group of bits containing the same number or fewer bits than the scrambling bit sequence; XOR-ing the sequential group of bits with corresponding bits of the scrambling bit sequence in parallel, thereby generating scrambled bits; and shifting the bits in the scrambling register by a number of spaces equal to the number of scrambled bits and subsequently transmitting and storing the scrambled bits in corresponding cells of the scrambling register in lowest ordinal sequence for use in subsequent XOR-ing of a next sequential group of bits.